

2014 CPMT Seminar

Latest Advances in Organic Interposers

APX (Advanced Package X) - Advanced Organic Technology for 2.5D Interposer



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THE NEW VALUE FRONTIER

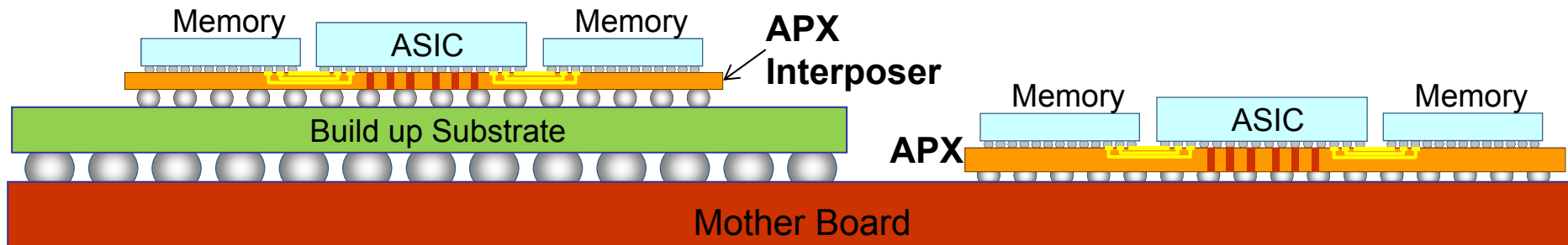


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▶ Agenda / Outline / Overview

- Benefits of 2.5D APX Interposer
- Technology Feature of APX
- Cross Section
- Design Rule Comparison
- Material Property
- Design Rule for Impedance Control
- Electrical Performance Study
- Routing Capability/Study
- Reliability Test Status
- Surface Finish Experience
- Technology Roadmap

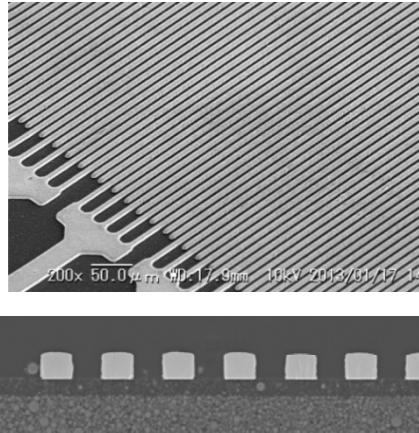
Benefits of 2.5D APX Interposer



《APX features and benefits》

- ◆ Fine pitch wiring and Small Size Via to support 2.5D interposer
- ◆ Plane pattern can be applied to POWER supply for lower IR Drop
- ◆ Z0 matching of Line, Via. and TH to 50Ω
- ◆ Smaller Signal transmission loss vs Silicon Interposer
- ◆ APX CTE is around 10ppm to strike a balance between 1st and 2nd assembly
- ◆ High stiffness by using high Young Modulus and Low CTE core for easy handling and assembly
- ◆ Open/short test can be done before APX is shipped
- ◆ Lower Cost potential vs Silicon Interposer or Glass interposer

Technology Feature of APX

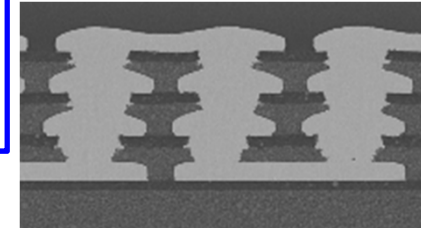


Fine Line/Space

Min. Line Width : 6um
Min. Space : 6um

Small Build Up VIA

Via Hole dia. : 20um
Via Land dia. : 32um
3 Stack



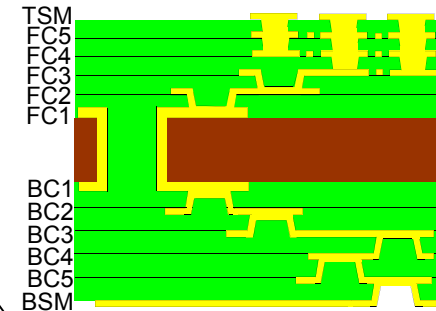
Micro bump pitch

32um 6um 6um

Min. 40um (experienced)
Min. 50um (a line escape between vias)

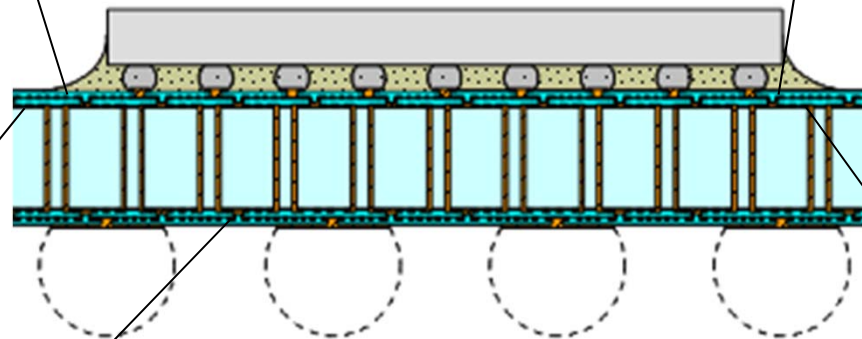


Max. Stack Up : 5-2-5



Fine Line/Space on Core (FC1/BC1)

Min. Line Width : 20um
Min. Space : 20um



Advanced Build-up Material

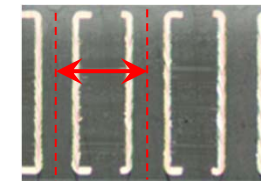
Ultra-Thin : 8um
Low Loss Tangent : 0.0066

Low CTE Organic Interposer

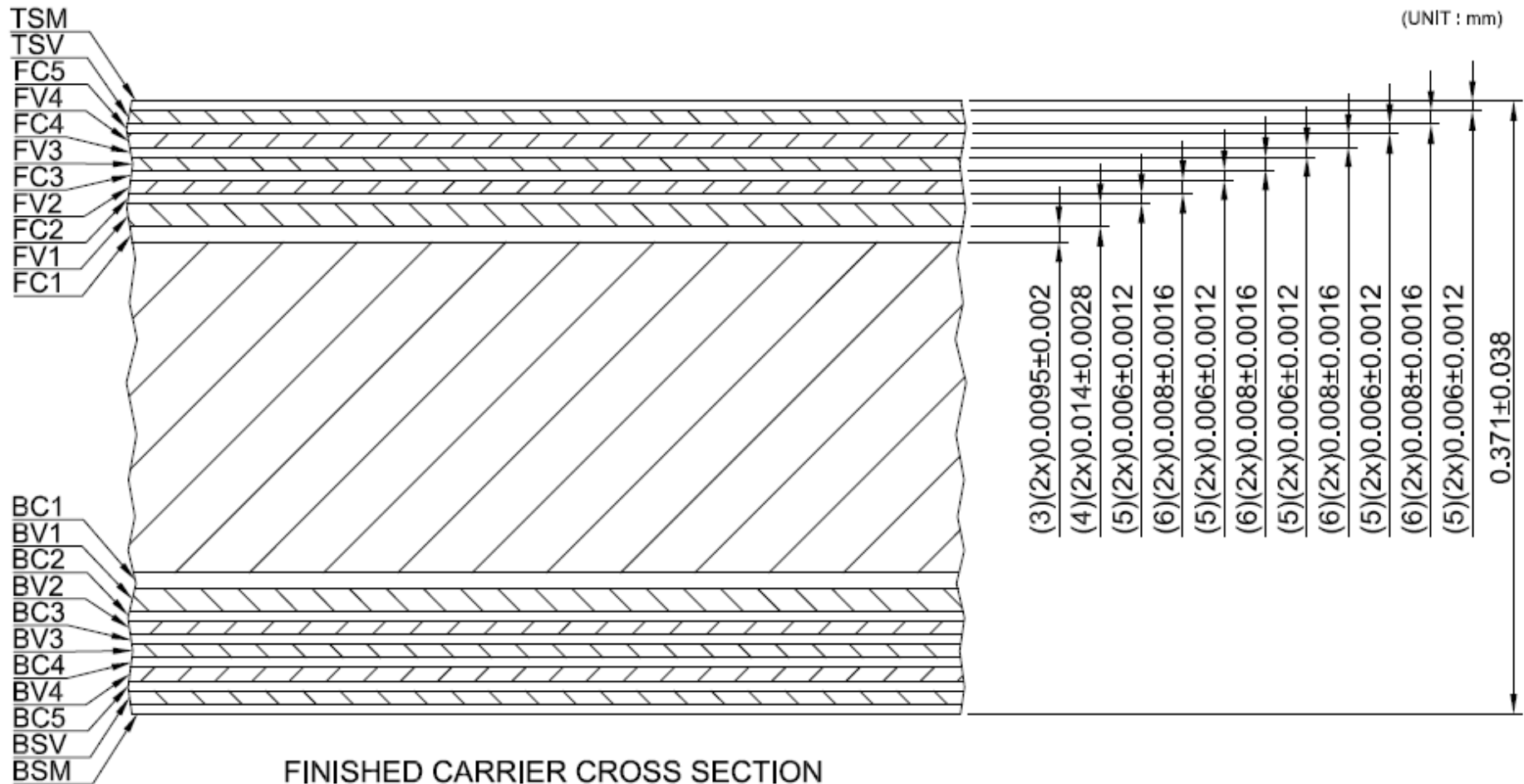
10~11 ppm (total)

Fine Pitch PTH

Pitch : 110um
Hole dia. : 60um
Land dia. : 80um

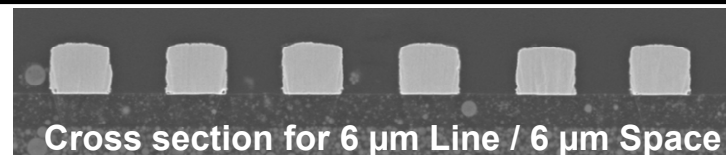


Cross Section of APX 5-2-5 Structure



Design rule Comparison

	ABF Build Up (most advanced)	APX
Min. Line Width (um)	9	6
Min. Space (um)	12	6
Via Hole Diameter (um)	65	20
Via Land Diameter (um)	85	32
Max. number of Via Stack	5	3
Build up Layer Thickness (um) (2 nd or above B/U Layer)	30	8
Max. build up layer	11	5
Max. Layer Count	24 (11-2-11)	12 (5-2-5)
PTH Pitch (um)	150	110



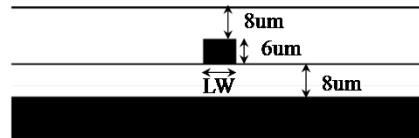
Material property

Item		ABF		APX	
		GX-13	GZ-41	Build Up (ZS-100) (Measured by KST with 10umt film)	CORE (Supplier's Catalogue Value)
Loss tangent		0.016/0.012 (1MHZ/1GHz)	0.0057/0.0058 (1MHZ/1GHz)	0.0063/0.0066 (2.8GHz/10GHz)	0.005 (1GHz)
Dielectric constant		3.6/3.35 (1MHZ/1GHz)	3.4/3.3 (1MHZ/1GHz)	3.1 / 3.1 (2.8GHz/10GHz)	4.0 (1GHz)
CTE x-y	TMA (ppm/degC)	46 (25-150degC)	20 (25-150degC)	28 (30-100degC)	4 (α1)
CTE z	TMA (ppm/degC)	47 (25-150degC)	20 (25-150degC)	28 (30-100degC)	12 (α1)
Tg	TMA (degC)	156	171	150	255 (by DMA)
Young's Modulus	Gpa	4.0	9.0	6.4-7.3	32 (@30degC)

Design Rule for Impedance Control by APX

Micro strip line

Single end



LW = 16.5um Z0 = 50 ohm

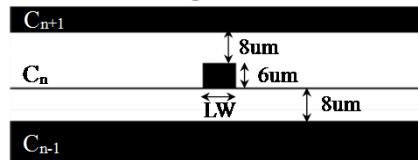
Differential pair



SP = 30.5um Zdiff = 100 ohm

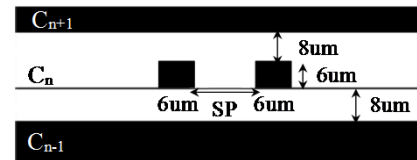
Strip line

Single end



LW = 7.5um Z0 = 50 ohm

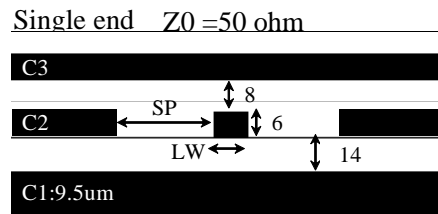
Differential pair



SP = 14.5um Zdiff = 100 ohm

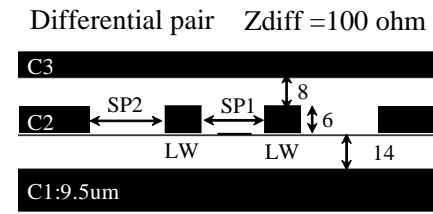
Strip line

Single end



LW = 10um SP = 19.5um
Z0 = 50 ohm

Differential pair

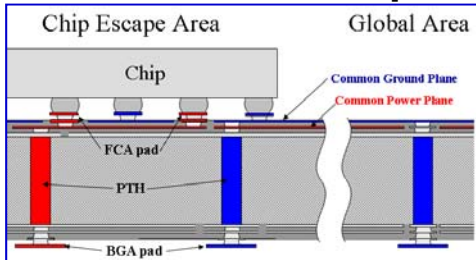


LW = 9um SP1 = 21um SP2 = 16um
Zdiff = 100 ohm

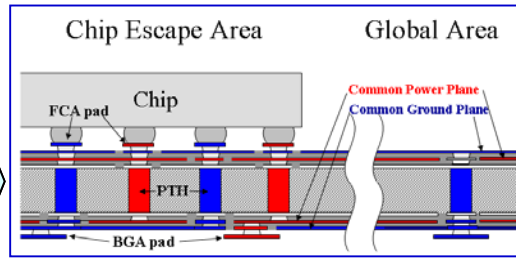
Electrical Performance Study

Loop Inductance Comparison

Current Build Up

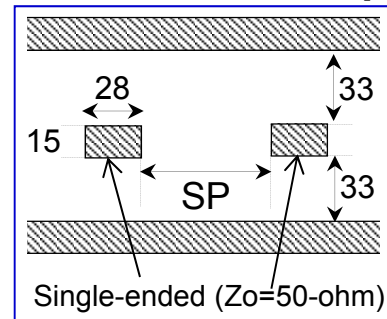


APX

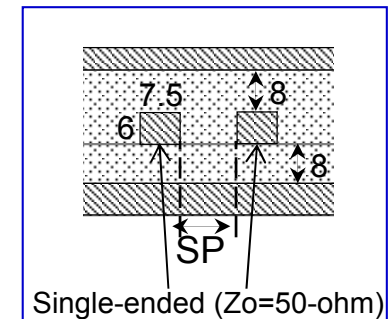


Cross Talk Noise Comparison

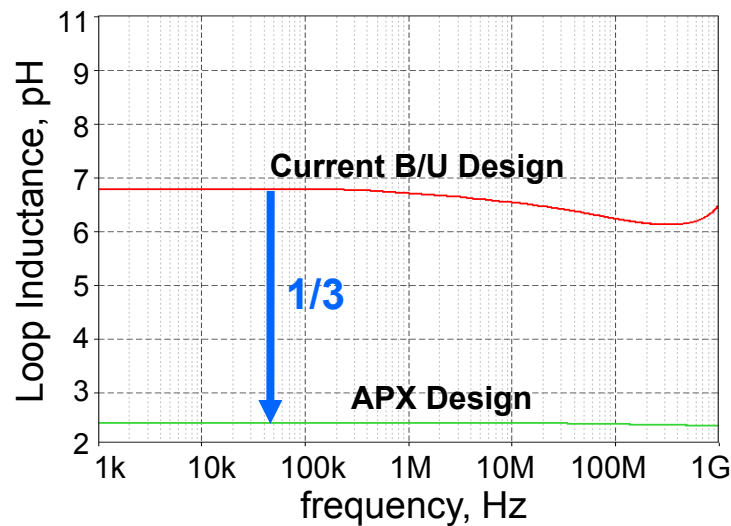
Current Build Up



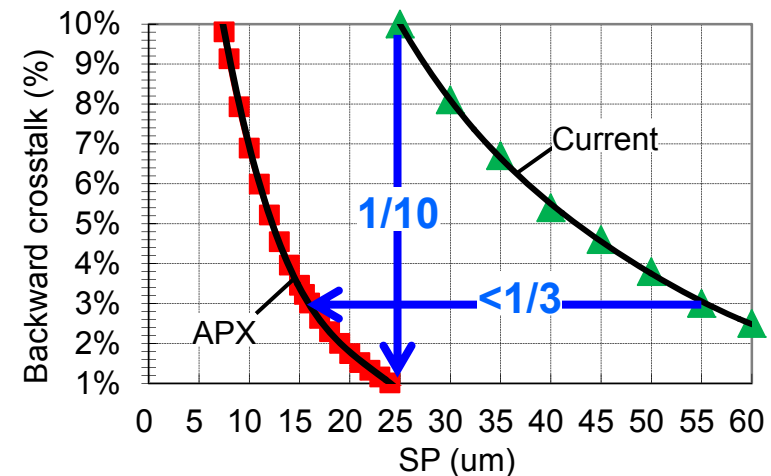
APX



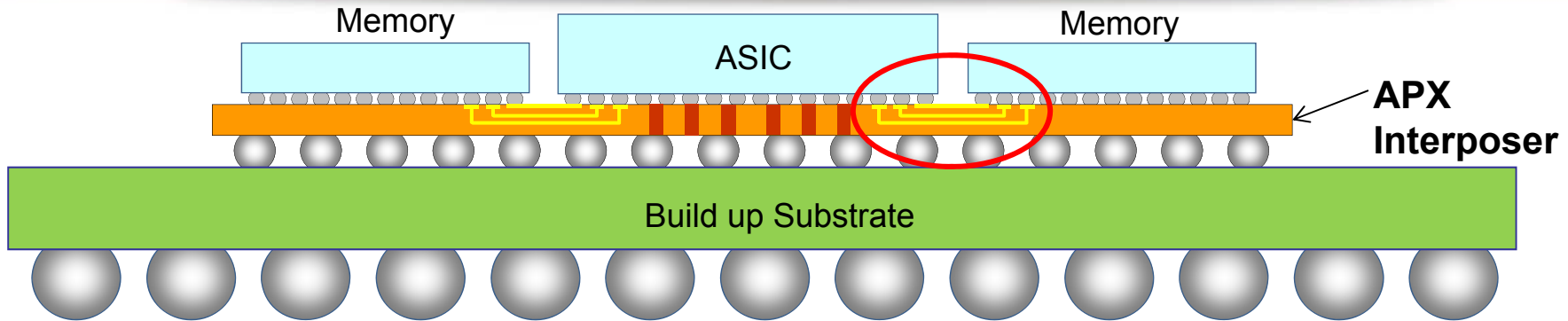
Loop Inductance Simulation Result



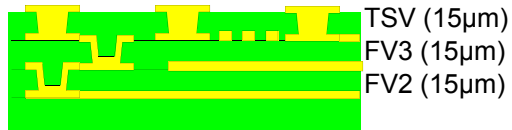
Cross talk noise Simulation Result



APX Routing Capability Study for 2.5D Package



120um pitch FCA



Wiring between Pads

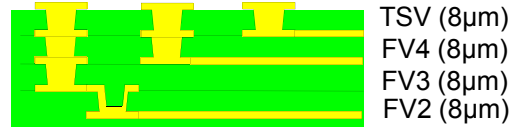
6 Line between vias

Pad dia. 32μm
L / S = 6μm / 6μm



50um pitch FCA (WB-DRAM)

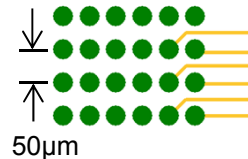
Via structure(4-2-4, 5-2-5)



Wiring between Pads

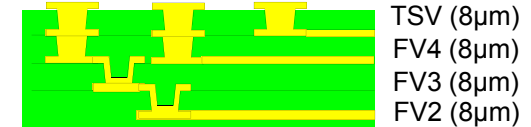
1 Line between pads

Pad dia. 32μm
L / S = 6μm / 6μm



55um pitch FCA (HBM)

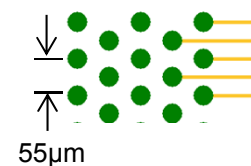
Via structure(5-2-5)



Wiring between Pads

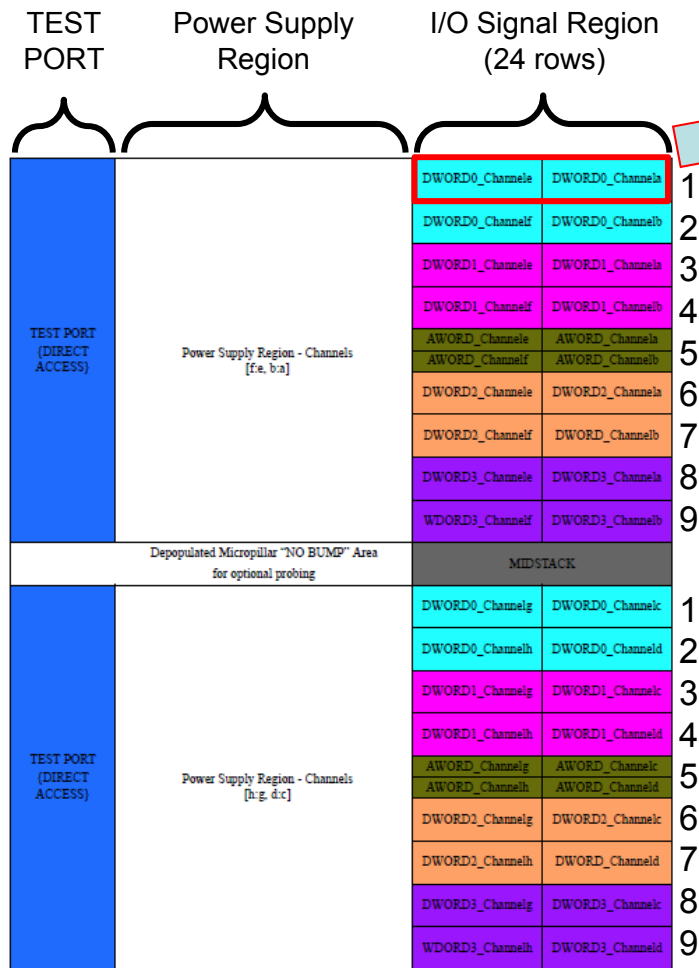
1 Line between pads

Pad dia. 32μm
L / S = 6μm / 6.5μm



HBM Ballout Map

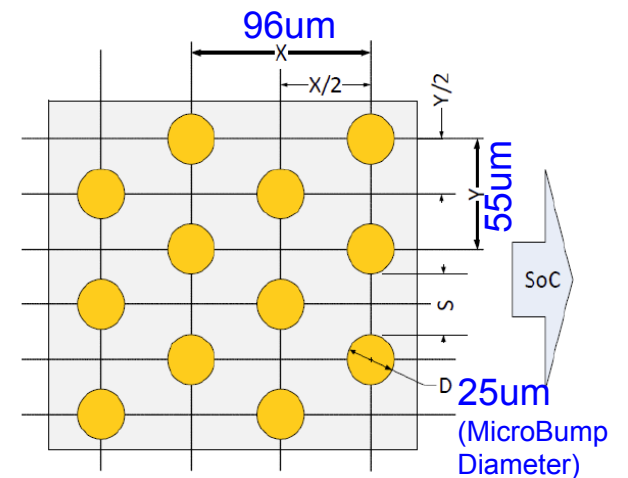
HBM Overall



I/O Signal Region

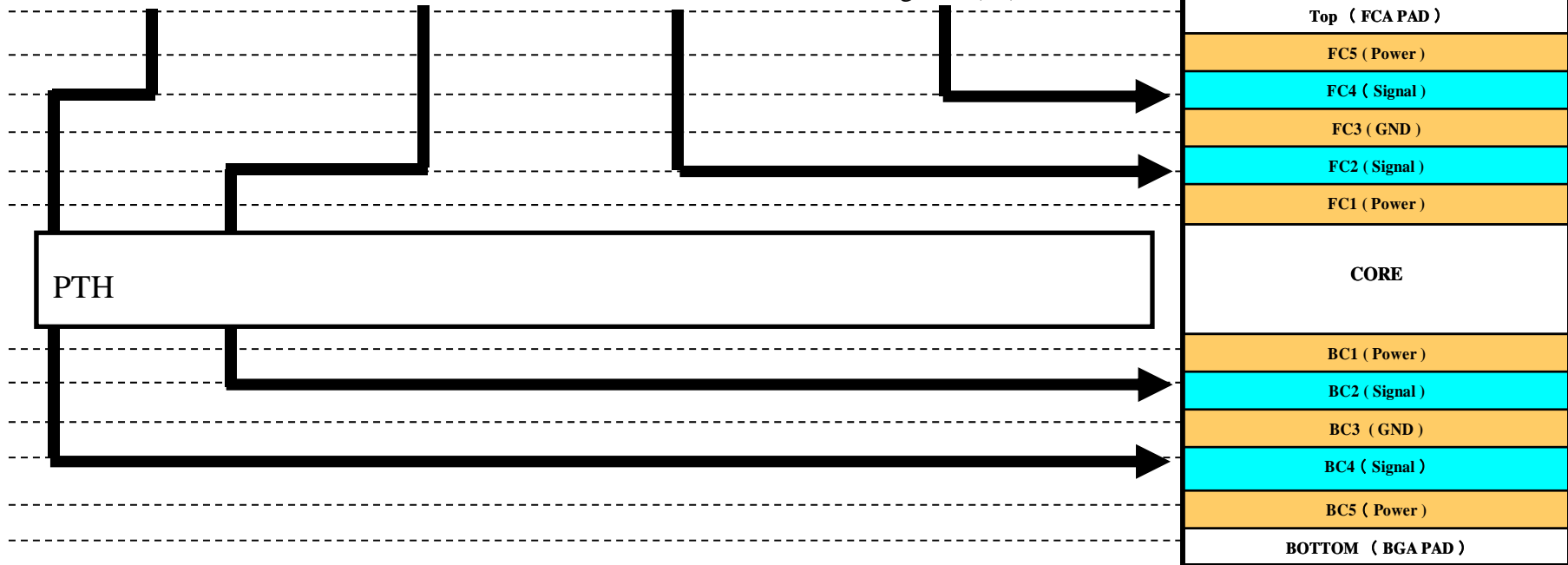
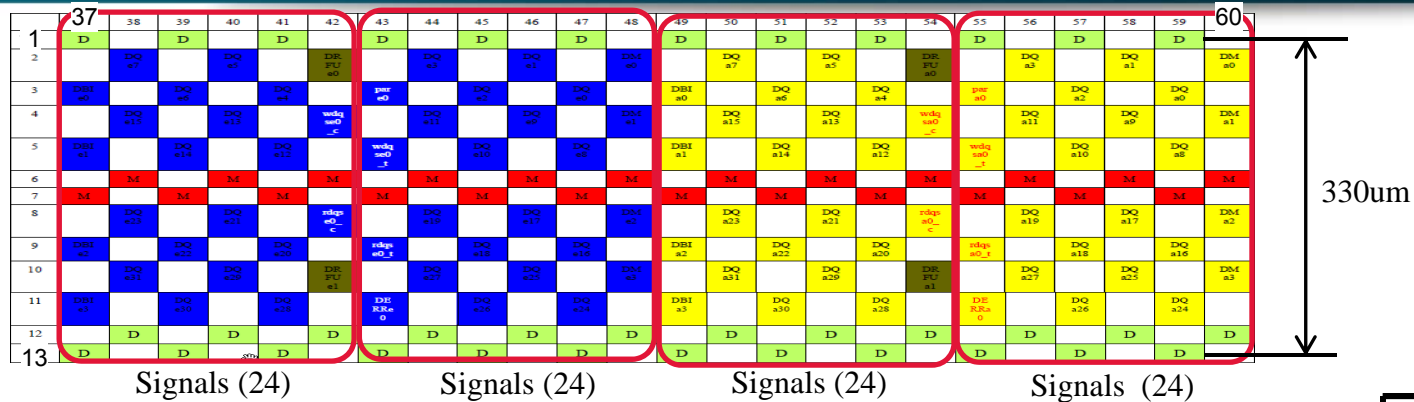
	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	
1	D		D		D		D		D		D		D		D		D		D		D		D		D
2		DQ a7		DQ a5		DR FU a6		DQ a4		DM a0		DQ a1		DQ a7		DQ a5		DR FU a6		DQ a3		DQ a1		DM a0	
3		DBI a0		DQ a2		DQ a1		DR FU a6		DQ a5		DQ a3		DBI a0		DQ a6		DQ a4		DR FU a6		DQ a2		DQ a0	
4		DQ a15		DQ a13		WDQ sa0_c		DQ a11		DQ a9		DM a1		DQ a15		DQ a13		WDQ sa0_c		DQ a11		DQ a9		DM a1	
5		DBI a1		DQ a14		DQ a12		WDQ sa0_f		DQ a10		DQ a8		DBI a1		DQ a14		DQ a12		WDQ sa0_f		DQ a10		DQ a8	
6		M		M		M		M		M		M		M		M		M		M		M		M	
7		M		M		M		M		M		M		M		M		M		M		M		M	
8		DQ a3		DQ a3		RDQS a0_c		DQ a19		DQ a17		DM a2		DQ a23		DQ a21		RDQS a0_c		DQ a19		DQ a17		DM a2	
9		DBI a2		DQ a21		DQ a20		RDQS a0_f		DQ a18		DQ a16		DBI a2		DQ a22		DQ a20		RDQS a0_f		DQ a18		DQ a16	
10		DQ a31		DQ a29		DR FU a1		DQ a27		DQ a25		DM a3		DQ a31		DQ a29		DR FU a1		DQ a27		DQ a25		DM a3	
11		DBI a3		DQ a30		DQ a28		DR Re 0		DQ a26		DQ a24		DBI a3		DQ a30		DQ a28		DR Re 0		DQ a26		DQ a24	
12		D		D		D		D		D		D		D		D		D		D		D		D	

VPP	A
NC	B
No Bump	C
VSS	D
VDDC	E
RSVD	
DA	
DRFU, ARFU, MRFU	
Test	
Temp	
RESET_n	L
VDDQ	M

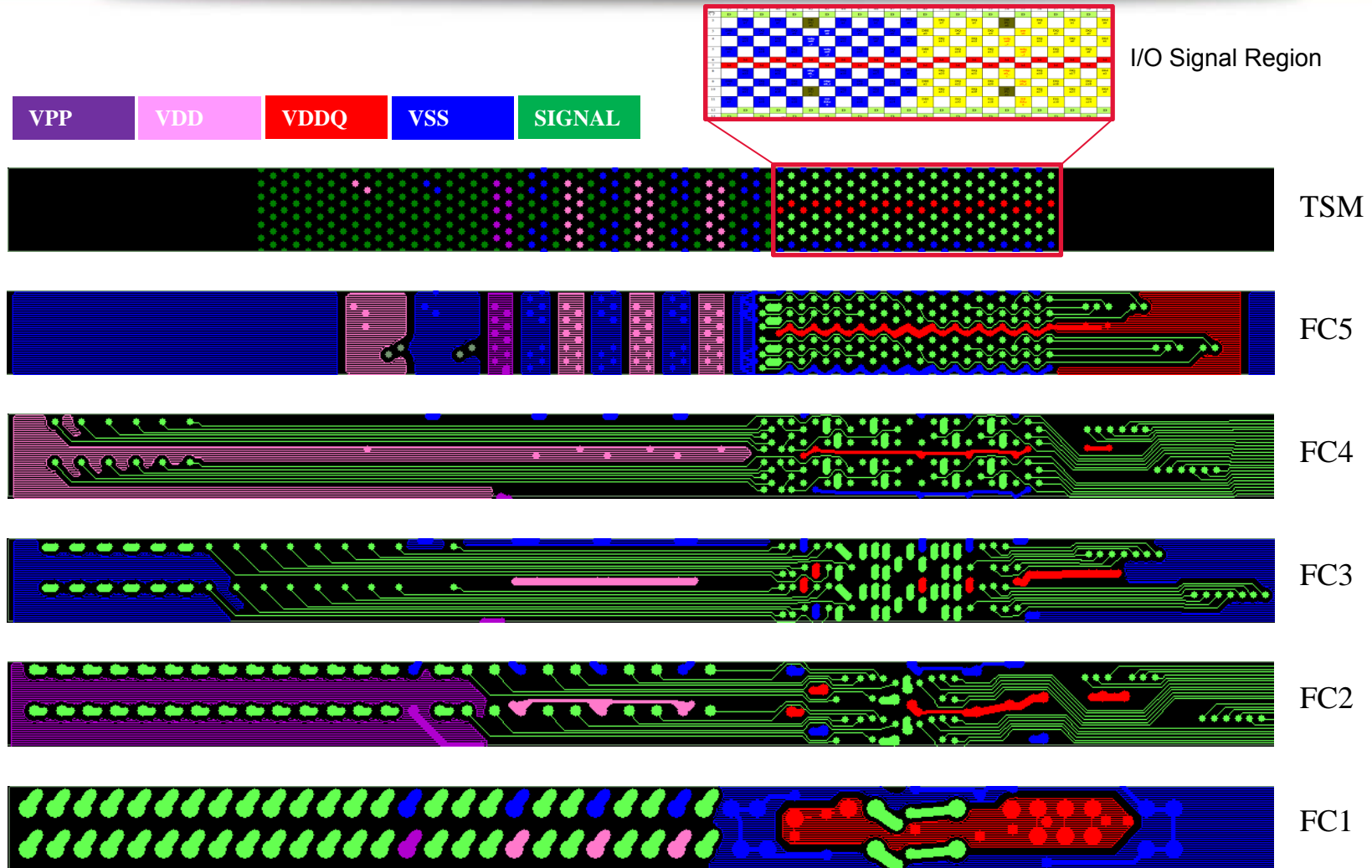


18 channels +MIDSTACK (220 columns)

Signal Fan-out Design Study from HBM



Signal Fan-out Design Study Result



All Signals can be fan-out !

Reliability Test Status

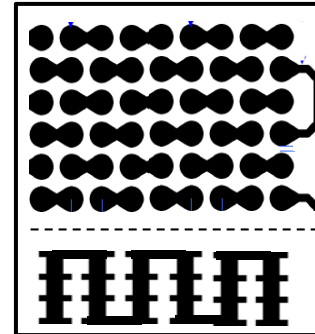
Substrate Level Reliability Test Status

Test Vehicle

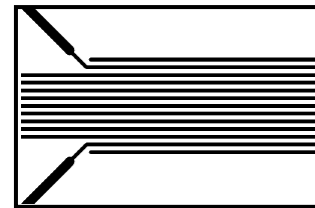
1. 3 Stacked VIA Chain
2. 6um Line width / 6um Line-to-Line -Space
3. 6um Line-to VIA_Land Space

Qualification Test Status

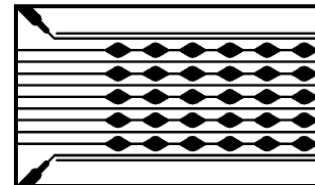
WTC (-65/150degC; 400cycles)	Passed
DTC (-55/125degC; 1000cycles)	Passed
HAST(130degC,85%,3.7V; 288hrs)	Passed
THB (85degC,85%,5V; 1000hrs)	under Testing



Risk site (3stacked via)
•40um pitch : 1,044vias/pcs
•50um pitch : 1,044vias/pcs
Total : 10,440vias(1,044x10)



Risk site (Line-Line)
•6um space : 198mm/pcs
Total : 1,782mm(198x9)



Risk site (Line - Land)
•6um space : 3,280pts/pcs
Total : 29,520pts(3,280x9)

Module Level Reliability Test Status

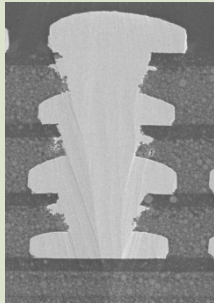
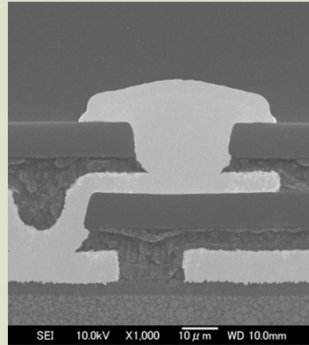
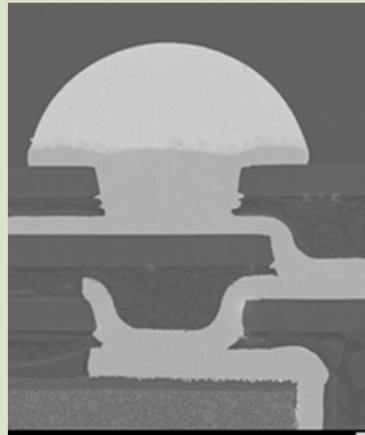
Test Vehicle

1. Dummy Chip Attached / No FCA Joint on 3 Stacked VIA Chain

Qualification Test Status

WTC (-65/150degC ; 400cycles)	Passed
DTC (-55/125degC ; 1000cycles)	Passed

Surface Finish Experience

	OSP	NiAu , NiPdAu	SAC (Solder)
Pad Pitch	> 40um	> 50um	> 150um
Pad-Pad Space	> 8um	> 18um	
	 <p>Gliccoat-SMD F2(PK) Entek Cu56</p>	 <p>* Reference picture</p>	 <p>* Reference picture</p>

APX Technology Roadmap

		CY 2013		CY 2014	CY 2015	CY2016	CY2017	
		~3Q	4Q~					
Substrate	CTE (ppm)	10-11	10-11	10-11	10-11	10-11	10-11	
					7 (target)	7 (target)	7 (target)	
	Size (mm) Depend on Build up L/S Depend on Equipment	≤93(12/12) ≤70(10/10)	≤93(12/12) ≤70(10/10) ≤30(6 / 6)	≤93(12/12) ≤70(10/10) ≤30(5 / 5)	≤77(5 / 5)	≤77	≤77	
Core	Core Layer	2	2	2	2	2	2	
	Min Line/ Space (um)	20/20	20/20	20/20	20/20	15/15	15/15	
	Core Thickness (um)	200	200	200	200	150 or 200	150 or 200	
	PTH Hole (um)	>50	>50	>50	T.B.D.	T.B.D.	T.B.D.	
	PTH Pitch (um)	≥150	≥110	≥100	≥100	≥80	≥80	
	PTH Land (um)	80	80	80	80	65	65	
Build Up	Build up Material	Polyimide	Epoxy	Epoxy	T.B.D.	T.B.D.	T.B.D.	
	Number of Build up Layer	4	5	5	3	3	3	
	Min. Line/ Space (um)	10/ 10	6/ 6	5/ 5	3/ 3	3/ 3	2/ 2	
	Conformal V1 via	Hole (um)	40/38	40/38	33	20	20	15
		Land (um)	50	50	50	32	32	25
	Filled Vn via	Hole (um)		20	20	15	15	13
		Land (um)		32	32	25	25	22
	Number of Via stack	0	3	3	2	2	2	

Update: May.2014

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